

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Appl. No.

09/849,005

Confirmation No.

1848

Technology Center 210

First Inventor

Chian-Min Richard Ho

Filing Date

May 4, 2001

Tech. Center/

2123

Examiner

Frejd, Russell Warren

Art Unit

Title:

Method for automatically searching for defects in a description of a circuit

Docket No.:

0IN006-1C US

Customer No.:

34036

Santa Clara, California October 20, 2003

COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, VA 22313-1450

## **LETTER**

## Dear Sir:

Attached hereto are three documents that were previously identified as references 9, 10 and 11 in the form PTO-1449 (part A) filed on October 10, 2003.

Also attached are the following two documents which were cited in the background section of the above-identified patent application:

"Hardware/Software Co-Design of the Stanford FLASH Multiprocessor", by Mark Heinrich, David Ofelt, Mark A. Horowitz, and John Hennessy, Proceedings of the IEEE, Vol 85, No. 3, pp. 455-466, March 1997; and "Functional Verification Methodology for the PowerPC 604 Microprocessor", by James Monaco, David Holloway and Rajesh Raina, Proceedings 33rd IEEE Design Automation Conference, pp. 319-324, June 1996.

No fee is believed to be required for consideration of the attached five documents because a fee was paid with the IDS filed October 10, 2003. If for any reason, any additional fees are required, Applicants respectfully request that a charge be made to the Deposit Account 50-2263 while referencing the Docket No. 0IN006-1C US.

Should the Examiner have any questions concerning this letter, the Examiner is invited to call the undersigned at (408) 982-8200, ext. 3.

Via Express Mail Label No. ER 205 700 331 US Respectfully submitted,

Omkar K. Suryadevara Attorney for Applicants

Reg. No. 36,320